REMARKS/ARGUMENTS

In response to the Office Action dated March 6, 2003, claims 13-15 are amended. Claims 6-15 remain in the application. It is not the Applicants' intent to surrender any equivalents because of the amendments or arguments made herein. Reexamination and reconsideration of the application, as amended, are respectfully requested.

Art-Based Rejections

In paragraphs 1-2 of the Office Action, claims 6-9, 11, and 14-15 were rejected under 35 U.S.C. § 102(b) as being anticipated by Omoya et al., USPN 5,641,996.

In paragraphs 3-4 of the Office Action, claim 10 was rejected under 35 U.S.C. § 103(a) as being anticipated by Omoya et al., USPN 5,641,996 in view of Matsuda et al., USPN 5,637,535.

In paragraph 5 of the Office Action, claim 12 was rejected under 35 U.S.C. § 102(b) as being anticipated by Omoya et al., USPN 5,641,996 in view of Fujiwara et al., USPN 4,735,847.

In paragraph 6 of the Office Action, claim 13 was rejected under 35 U.S.C. § 102(b) as being anticipated by Omoya et al., USPN 5,641,996 in view of Kushima et al., USPN 4,503,597.

The Applicant respectfully traverses the rejections in light of the arguments below.

The Omoya Reference

The Omoya reference discloses a semiconductor unit package and method.

At step ST3, as shown in FIGS. 4(a)-4(c), the semiconductor device 1, with the side of the stud bump electrode 14 facing down, is placed above a substrate 20 with application of a conductive adhesive 4a. Thereafter, the semiconductor device 1 is lowered towards the substrate 20 such that the stud bump electrode 14 is soaked in the conductive adhesive 4a on the substrate 20. Subsequently, the semiconductor device 1 is lifted up, as a result of which transfer of the conductive adhesive 4a onto the stud bump electrode 14 is completed.

Next, at steps ST4 and ST5, as shown in FIG. 4(d), the semiconductor device 1 is placed onto the ceramic substrate 6 having thereon the terminal electrode 5. At this time, alignment of the stud bump electrode 14 of the semiconductor device 1 with the terminal electrode 5 of the substrate 6 is carried out, and the conductive adhesive 4a is heated to cure to form the conductive adhesive layer 4. As a result, the stud bump electrode 14 of the semiconductor device 1 and the terminal electrode 5 of the substrate 6 are electrically connected together. See Col. 9, line 58-Col. 10, line 10.

The Matsuda Reference

The Matsuda reference discloses a semiconductor device with reliable electrodes of projecting shape. In this embodiment, as shown in FIG. 28, the assembly board 53 is attached in advance to a testing socket 61 which is connected to a testing device 60 for testing the semiconductor chip 51. In FIG. 29, the semiconductor chip 51 is connected to the assembly board 53 so as to connect the electrode pins 52 with the electrode pads 58. Since the electrode pads 58 are coupled

to the external-connection pins 53a, the semiconductor chip 51 is coupled to the testing device 60 via the assembly board 53 and the testing socket 61. In this positioning, the testing device 60 carries out a predetermined test on the semiconductor chip 51. See Col. 14, lines 12-25.

The Fujiwara Reference

The Fujiwara reference discloses an electrically conductive adhesive sheet. An oxide transparent conductive film (thickness of 1000.ANG.) formed of composite oxide composed of indium oxide and tin oxide was patterned on a transparent glass substrate to provide transparent striped electrode patterns as arranged in parallel relation with each other. On the other hand, a copper foil of 18 microns thickness formed on a polyimide flexible substrate of 25 microns thickness was etched by a photolithography method to form striped conductive track patterns corresponding to external lead connections of the above transparent conductive film. In this case, each of pitches of the transparent electrode patterns and the conductive track patterns was set to 0.4 mm (pattern width of 0.2 mm; pattern spacing of 0.2 mm). See Col. 13, lines 28-41.

The Kushima Reference

The Kushima reference discloses a method of forming a number of solder layers on a semiconductor wafer. Kushima is cited as disclosing solder foil in a net-like structure. See Col. 2, lines 48-49.

The Claims are Patentable over the Cited Reference

The claims of the present invention describe a method for preventing electrostatic damages to a semiconductor chip package during storage. A method in accordance with the present invention comprises forming one or more conductive members electrically connecting the terminals to each other; and disabling the electrical connections by an action of mounting the package on a printed circuit board.

The cited references do not teach nor suggest the limitations of the claims of the present invention. Specifically, the cited references does not teach nor suggest at least the limitation of disabling the electrical connections by an action of mounting the package on a printed circuit board as recited in the claims of the present invention.

The primary Omoya reference discloses disabling the electrical connections of the conductive adhesives 4a by separating semiconductor device 1 from the substrate 20. See Col. 9, lines 60-62. The separation of the semiconductor device 1 from the substrate 20, rather than the mounting of the semiconductor device 1 to the substrate 20, performs the disabling. This is in direct contrast to the claims of the present invention, where the mounting of the package onto a printed circuit board performs the disabling of the electrical connections. It is respectfully submitted that the Omoya reference teaches away from the claims of the present invention, and that claim 6 is patentable over the Omoya reference.

The ancillary Matsuda, Fujiwara, and Kushima references do not remedy the deficiencies of the Omoya reference. Specifically, none of the references, alone or in combination, teach or suggest at least the limitation of disabling the electrical

connections by an action of mounting the package on a printed circuit board as recited in the claims of the present invention.

Thus, it is submitted that independent claim 6 is patentable over the cited references. Claims 7-15 are also patentable over the cited references, not only because they contain all of the limitations of the independent claim, but because claims 7-15 also describe additional novel elements and features that are not described in the prior art.

Conclusion

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6742 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
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